

Appl. No. : 10/809,566  
Filed : March 25, 2004

### REMARKS

Claim 6 is amended herein. The amendment is supported by the specification, for example, at page 16, lines 17-24. No new matter is added by the amendment.

Applicants thank the Examiner for review of the instant application. Upon entry of the amendment, Claims 6 and 8 are presented for examination.

### Rejection of Claim 6 under 35 U.S.C. §103

Claim 6 is rejected under 35 U.S.C. §103, as being obvious over Nishiyama (U.S. Pub. No. 2002/0004288) in view of Jiang *et al.* (U.S. Pat. No. 6,812,064).

Claim 6, as amended, is directed to a method for manufacturing a semiconductor device, comprising steps of: providing a semiconductor wafer having a ground or polished surface activated in a grinding or polishing step, with semiconductor circuits formed thereon; cleaning the ground or polished surface with water; after the cleaning step, deactivating the ground or polished surface by blowing ozone on the ground or polished surface of the semiconductor wafer; adhering a dicing sheet to the deactivated ground or polished surface of the semiconductor wafer after; and dicing the dicing sheet-adhered wafer.

The Advisory Action states:

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Nishiyama by blowing ozone on the ground or polished surface of the semiconductor wafer as being claimed, per taught by Jiang, **to provide a clean semiconductor wafer by preventing the semiconductor wafer from picking unwanted contaminant** for a better manufacturing semiconductor device process.

\*\*\*

In regarding to Applicant's argument that it is not obvious to combine the teaching of Jiang to the Nishiyama process since Nishiyama does not suggest that cleaning the wafer should be performed by chemical modifying. The argument is not persuasive since **Examiner combines the teaching of Jiang based on deactivating step not cleaning by removing unwanted matter.** *Advisory Action* at pages 3, 4 (emphasis added).

In view of the above, the PTO's position on why one of ordinary skill in the art would combine the references is unclear – the Advisory Action's first assertion is that the motivation would be to clean the semiconductor wafer, and the Advisory Action's second assertion is that

Appl. No. : 10/809,566  
Filed : March 25, 2004

the motivation would be based on deactivating, not cleaning. In view of the ambiguity, Applicants address both asserted motivations.

### **Deactivating**

The Advisory Action states that “Nishiyama substantially discloses the claimed method including deactivating the ground or polished surface of the semiconductor wafer;” however, this alleged teaching of deactivating is based on Nishiyama’s teaching of cleaning the semiconductor wafer, which “would inherently deactivate the ground or polished surface of the semiconductor wafer.” *Advisory Action* at page 2. In particular, Nishiyama teaches:

FIG. 11A shows an LSI wafer 61 with its device surface 62 facing upward, which has normally a thickness of 600 .mu.m to 700 .mu.m. FIG. 11B shows the LSI wafer 61 having a protection sheet 63 pasted on its device surface 62. FIG. 11C shows the LSI wafer 61 which was ground and polished on its bottom surface 68 in order to reduce its thickness. After grinding and polishing to reduce the thickness, the LSI wafer 61 is **subjected to a cleaning process**, however, at this time, a delicate handling and care must be taken (when peeling off the protection sheet 63 or handling of the LSI wafer 61) lest a very thin LSI wafer 61 should be broken.

Next, in FIG. 11D, the protection sheet 63 is peeled off from the LSI wafer 61, and a dicing sheet 64 is pasted on a bottom surface 68 thereof. Further, FIG. 11E shows a step of fabricating LSI chips 65 through a dicing process by dicing the LSI wafer 61 into respective chips. By way of example, there is a problem that a crack tends to occur easily when the thickness of the LSI chip 65 which was ground becomes thinner at the time of dicing of the LSI wafer 61. *Nishiyama* at paragraphs [0015]-[0016].

Nishiyama never teaches or suggests deactivation of a semiconductor wafer. Accordingly, Nishiyama provides no reason for one skilled in the art to include a step of deactivation of the semiconductor wafer in the method of Nishiyama. The mere possibility that some cleaning processes may inherently result in inactivating the semiconductor wafer cannot provide motivation to one skilled in the art to specifically include a step of deactivation in the method of Nishiyama because nothing in Nishiyama remotely suggests the desirability of deactivating a semiconductor wafer. Moreover, Nishiyama does not teach or suggest that cleaning the wafer or any other process step would include chemically modifying (*i.e.*, oxidizing with ozone) the semiconductor wafer surface. Nishiyama provides no reason whatsoever for considering that any process step should involve modifying the ground semiconductor wafer

**Appl. No.** : **10/809,566**  
**Filed** : **March 25, 2004**

surface. If anything, Nishiyama's teaching of "cleaning" a semiconductor wafer should be viewed as removing unwanted matter, and not as chemically modifying the semiconductor wafer surface. Thus, in its plain meaning, Nishiyama's teaching of "cleaning" a semiconductor wafer would discourage one of ordinary skill in the art from performing an additional deactivating step to chemically modify the semiconductor wafer surface. Accordingly, Nishiyama's teachings would encourage one of ordinary skill in the art to avoid deactivating the semiconductor wafer after cleaning the ground semiconductor wafer surface.

Even if the cleaning step of Nishiyama was modified to result in chemically modification to the semiconductor wafer, such a modification to the method of Nishiyama would not render obvious the method of Claim 6 as presently claimed because Claim 6, as amended, recites separate steps of cleaning the ground or polished surface of the semiconductor wafer with water, and after the cleaning step, deactivating the ground or polished surface by blowing ozone on the ground or polished surface of the semiconductor wafer. Nothing in Nishiyama would lead one of ordinary skill to first clean a semiconductor wafer surface, and then, separately and subsequently, to deactivate the semiconductor wafer surface.

Regarding the teachings of Jiang, the Advisory Action points to three locations in Jiang for teaching that the benefit of having a silicon dioxide layer on the semiconductor wafer is to decrease unwanted sticking of pick-up tips to the ground wafer during robotic transfer operations. However, modification of Nishiyama to add a step of deactivating the wafer would serve no purpose since Nishiyama teaches pasting a dicing sheet on the bottom surface of the cleaned wafer, which would serve to prevent the sticking of the wafer to the robotic pick-up tips. *Nishiyama* at paragraph [0016]. Accordingly, Jiang provides no basis for adding a further step to the method of Nishiyama because forming a silicon dioxide layer on a semiconductor wafer pasted to a dicing sheet would not further prevent the sticking of the wafer to the robotic pick-up tips beyond the prevention afforded by the dicing sheet.

Furthermore, no combination of the cited references teaches or suggest separate steps of both cleaning the ground or polished surface of the semiconductor wafer with water, and deactivating the ground or polished surface by blowing ozone on the ground or polished surface of the semiconductor wafer, much less the order of these steps. There is no indication from either reference that first cleaning the semiconductor wafer surface and then deactivating the semiconductor wafer surface would provide any particular benefit. For example, there is no

**Appl. No.** : **10/809,566**  
**Filed** : **March 25, 2004**

reason provided in Jiang that cleaning the wafer prior to forming a silicon dioxide layer would provide any particular benefit to inhibiting the sticking of pick-up tips to the semiconductor wafer, even if one were to avoid using the dicing sheet taught in Nishiyama. In contrast to the teachings of the cited references, blowing ozone after cleaning in accordance with the presently claimed method, avoids the possibility of not successfully ozone-treating the entire semiconductor wafer surface. If the wafer back surface treating method does not include cleaning process before blowing ozone, for example, the portion covered with dust will not be ozone-treated. The method of Claim 6, as amended, will avoid undesired results like this.

In contrast to Nishiyama and Jiang, Applicants have found that, by adhering a dicing sheet to a ground or polished surface of a semiconductor wafer after a deactivation treatment applied on the ground or polished surface thereof activated in a grinding or polishing step, dicing can be conducted in a state where a sticking force therebetween is reduced. By incorporating this deactivation treatment step, after-dicing methods such as picking up of semiconductor chips to which a dicing sheet is adhered is facilitated, and contamination of the semiconductor chips by the dicing sheet is inhibited (see, e.g., Table 1).

Nishiyama and Jiang, alone or combined, do not teach any problems associated with adhering a dicing sheet to a ground or polished semiconductor wafer. Nishiyama and Jiang, alone or combined, provide no motivation to one of ordinary skill in the art to adhere a dicing sheet to a ground surface of a wafer after deactivation treatment and prior to dicing. As such, Nishiyama and Jiang, alone or combined, do not teach or suggest the method of Claim 6. In view of the amendments to Claim 6 and the above remarks, Applicants respectfully request removal of the obviousness rejection of Claim 6.

### **Cleaning**

While Applicants maintain for reasons previously of record that one of ordinary skill in the art would not have been motivated to “clean” the semiconductor wafer of Nishiyama by chemically modifying the semiconductor wafer using the method of Jiang, Applicants submit that the amendment to Claim 6 renders the Advisory Action’s asserted motivation of cleaning the semiconductor wafer moot because the presently claimed method of Claim 6 recites separate steps of cleaning the ground or polished surface of the semiconductor wafer with water, and after

**Appl. No.** : 10/809,566  
**Filed** : March 25, 2004

the cleaning step, deactivating the ground or polished surface by blowing ozone on the ground or polished surface of the semiconductor wafer.

Since the alleged motivation to modify the method of Nishiyama with the method of Jiang is to clean the semiconductor wafer surface, it would make no sense to clean the semiconductor wafer surface in a first step, and in a separate, second step, deactivate the semiconductor wafer surface by blowing ozone. If the purpose of using the method of Jiang would be to clean the semiconductor wafer surface, no combination of these references would motivate one of ordinary skill to perform separate cleaning and deactivation steps.

In contrast to the teachings of the cited references, blowing ozone after cleaning according to the presently claimed method, avoids the possibility of not successfully ozone-treating the entire semiconductor wafer surface. If the wafer back surface treating method does not includes cleaning process before blowing ozone, for example, the portion covered with dust will not be ozone-treated. The method of Claim 6, as amended, will avoid undesired results like this.

In contrast to Nishiyama and Jiang, Applicants have found that, by adhering a dicing sheet to a ground or polished surface of a semiconductor wafer after a deactivation treatment applied on the ground or polished surface thereof activated in a grinding or polishing step, dicing can be conducted in a state where a sticking force therebetween is reduced. By incorporating this deactivation treatment step, after-dicing methods such as picking up of semiconductor chips to which a dicing sheet is adhered is facilitated, and contamination of the semiconductor chips by the dicing sheet is inhibited (see, e.g., Table 1).

Nishiyama and Jiang, alone or combined, do not teach any problems associated with adhering a dicing sheet to a ground or polished semiconductor wafer. Nishiyama and Jiang, alone or combined, provide no motivation to one of ordinary skill in the art to adhere a dicing sheet to a ground surface of a wafer after deactivation treatment and prior to dicing. As such, Nishiyama and Jiang, alone or combined, do not teach or suggest the method of Claim 6. In view of the amendments to Claim 6 and the above remarks, Applicants respectfully request removal of the obviousness rejection of Claim 6.

#### **CONCLUSION**

**Appl. No.** : **10/809,566**  
**Filed** : **March 25, 2004**

In view of the above, Applicants respectfully maintain that claims are patentable and request that they be passed to issue. Applicants invite the Examiner to call the undersigned if any remaining issues may be resolved by telephone.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: December 19, 2006

By: 

Kerry Taylor  
Registration No. 43,947  
Agent of Record  
Customer No. 20,995  
(619) 235-8550

3216291  
121506